

AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED

REVISION TO 37 CFR 1.121)

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sub C1* 1. (ORIGINAL) An apparatus comprising:

a wireless transceiver coupled to a programmable logic circuit, wherein said programmable logic circuit comprises a programmable logic device, a processor, and a memory circuit in a
5 single integrated circuit (IC) package.

2. (ORIGINAL) The apparatus according to claim 1, wherein said single integrated circuit package contains one or more integrated circuit dies.

3. (ORIGINAL) The apparatus according to claim 1, wherein said integrated circuit comprises a JEDEC standard integrated circuit package.

4. (ORIGINAL) The apparatus according to claim 1, wherein said wireless transceiver is contained within said package.

5. (ORIGINAL) The apparatus according to claim 1, wherein said wireless transceiver communicates using either electromagnetic or ultrasonic waves.

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6. (ORIGINAL) The apparatus according to claim 5,
wherein said electromagnetic waves comprise radio signals or
infrared light.

7. (ORIGINAL) The apparatus according to claim 1,
wherein said wireless transceiver communicates through a device
selected from the group consisting of an antenna, a light
emitting/sensitive device, and an ultrasonic transducer.

8. (ORIGINAL) The apparatus according to claim 7,
wherein said light emitting/sensitive device comprises an infrared
diode or other type or wavelength of light emitting/sensitive diode
or transistor.

9. (PREVIOUSLY AMENDED) The apparatus according to
claim 1, wherein said processor and said programmable logic device
are implemented on a single die.

10. (ORIGINAL) The apparatus according to claim 1,
wherein said processor is selected from the group consisting of a
microprocessor, a micro-controller or other processor, a digital
signal processor, and instructions stored in said memory circuit
for configuring said programmable logic circuit as a processor.

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11. (ORIGINAL) The apparatus according to claim 10, wherein said instructions configure said programmable logic device as a device selected from the group consisting of a microprocessor, a micro-controller, and a digital signal processor.

12. (ORIGINAL) The apparatus according to claim 1, wherein said memory circuit comprises one or more non-volatile memory elements.

13. (ORIGINAL) The apparatus according to claim 1, wherein said programmable logic device comprises one or more memory elements.

14. (ORIGINAL) The apparatus according to claim 13, wherein said memory elements are non-volatile.

15. (ORIGINAL) A method for programming a programmable logic device using a wireless link comprising the steps of:

(A) presenting programming signals to a wireless transceiver; and

5 (B) programming a programmable logic circuit in response to said programming signals, wherein said programmable logic circuit comprises a programmable logic device, a memory circuit, and a processor in a single integrated circuit package.

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16. (ORIGINAL) The method according to claim 15,
wherein said wireless transceiver is contained in said integrated
circuit package.

17. (PREVIOUSLY AMENDED) The method according to claim
15, further comprising the steps of:

(C) during a first bootup, configuring said programmable
logic device as said processor in response to instructions stored
5 in said memory circuit; and

(D) reprogramming said memory circuit in response to
said programming signals.

18. (ORIGINAL) An apparatus comprising:
a programmable logic device;
a memory circuit;
a processor; and
5 a wireless transceiver, wherein said programmable logic
device, said memory circuit, and said processor are encased in a
single integrated circuit (IC) package.

19. (ORIGINAL) The apparatus according to claim 18,
wherein said wireless transceiver is contained within said
integrated circuit package.

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20. (ORIGINAL) The apparatus according to claim 18,
further comprising a transducer coupled to said wireless
transceiver.
